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Leading Innovation

New channel engineering for the low power CMOS technology

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Toshiba Corporation

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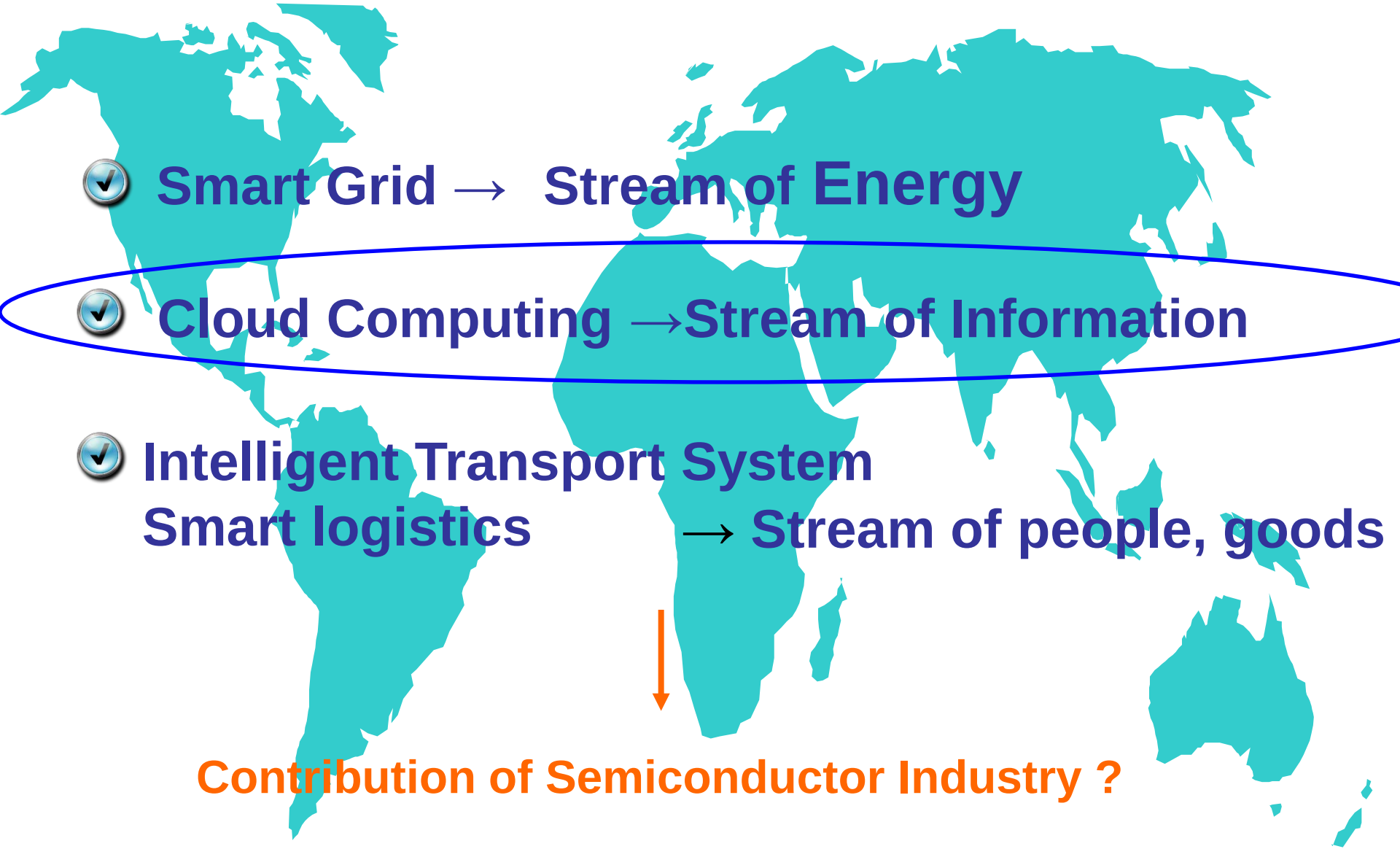
SMART Community: 3 Major Streams



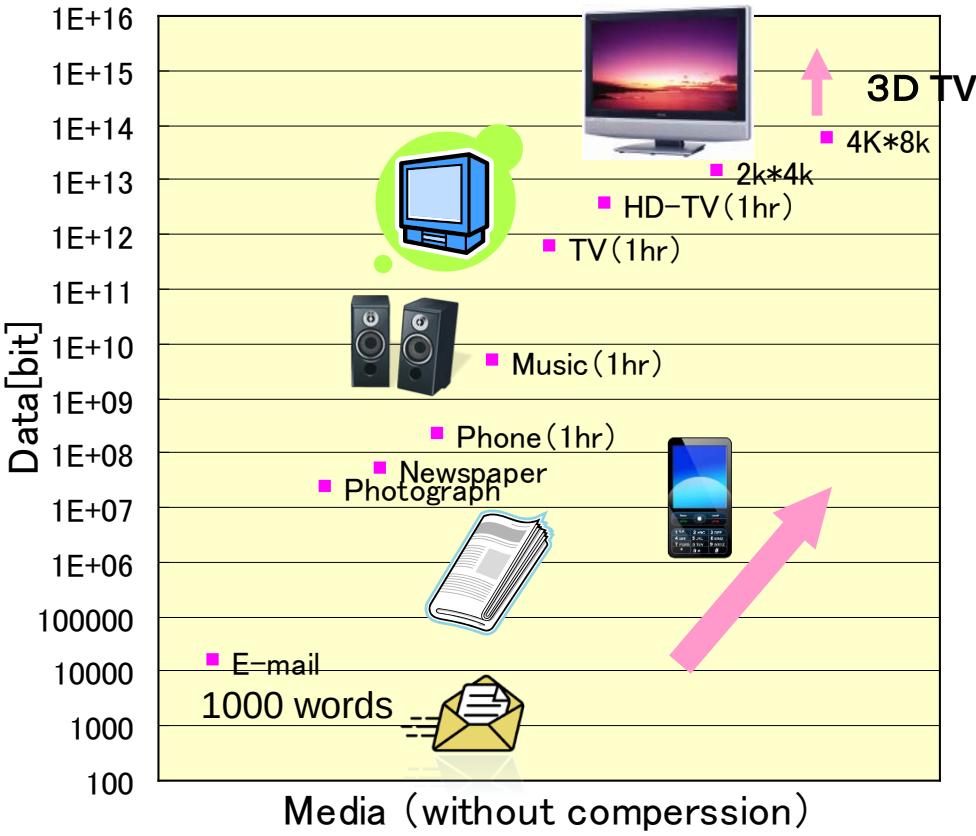
- **Smart Grid → Stream of Energy**
- **Cloud Computing →Stream of Information**
- **Intelligent Transport System**
  Smart logistics → Stream of people, goods

Contribution of Semiconductor Industry ?

*** Intelligent Transport System**

Explosion of Information

Data Center of Apple (50,000m^2)
(P.30, Bussinessweek Sept.6, 2010)



Larger Data Files

X

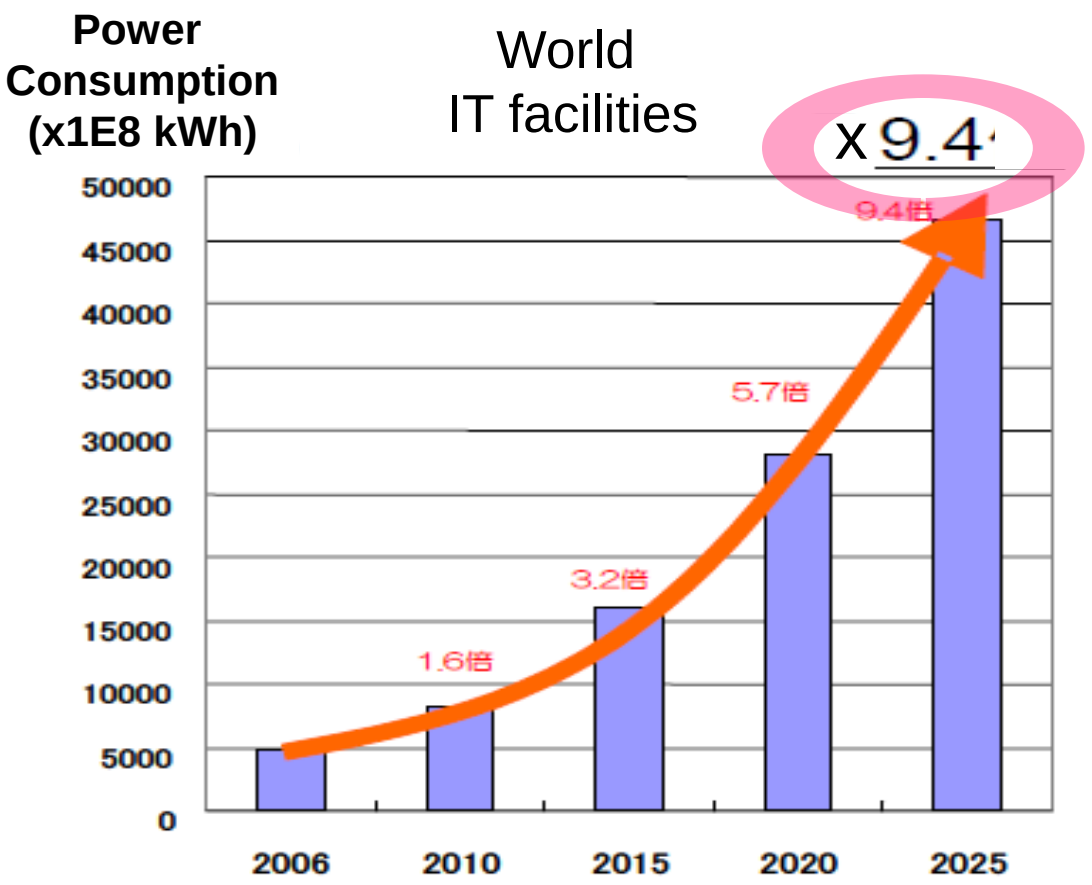
More Frequent Access

II

- **High Speed Processing**
- **Large data capacity with low cost**

Social Demands

Power Consumption increase for IT facilities



15% of world total power

Source: METI Japan
http://www.meti.go.jp/committee/materials/downloadfiles/g80520c03j.pdf

Large Power Consumption by IT facilities
→ Measures for Dramatic Energy Saving Requested.

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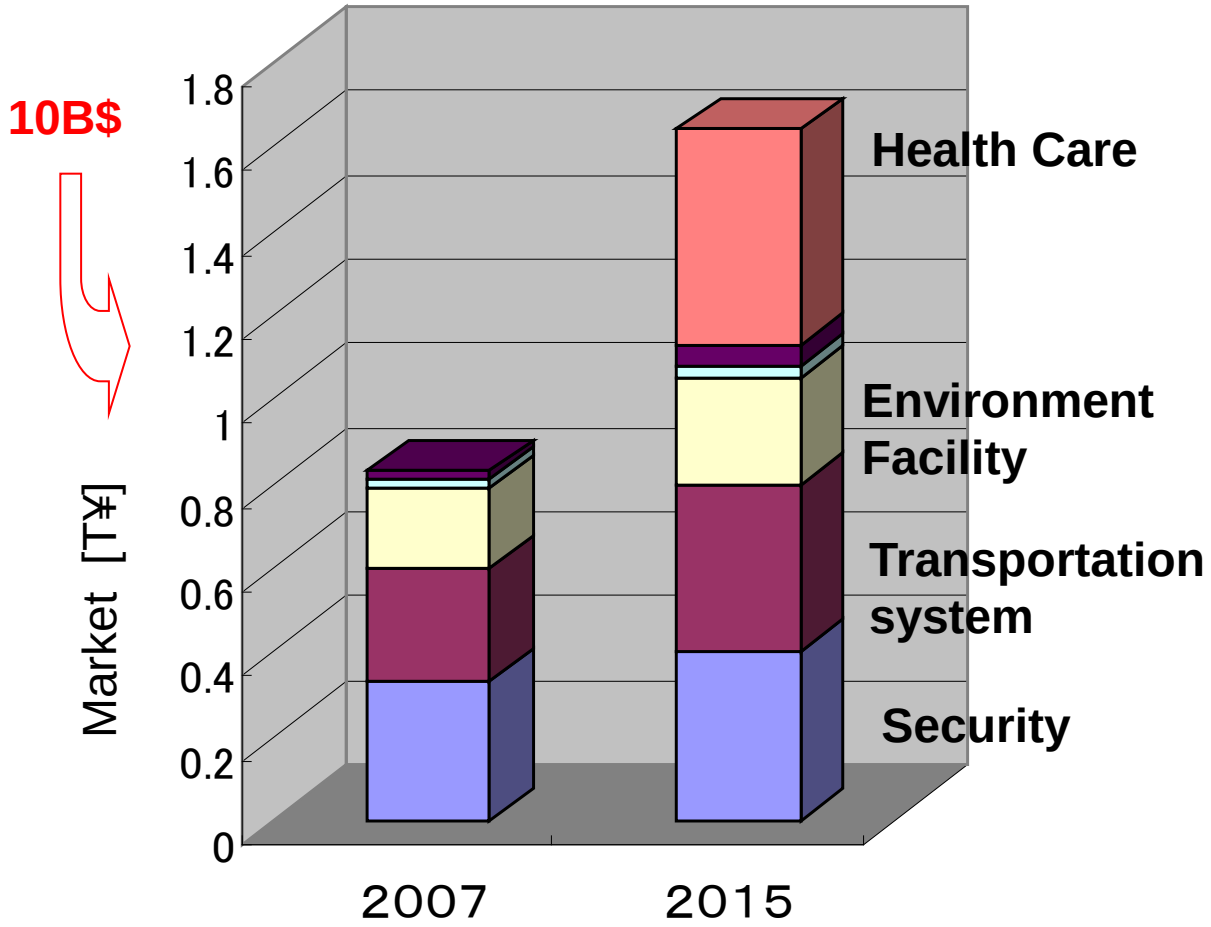
Sensor Network Market inside Japan

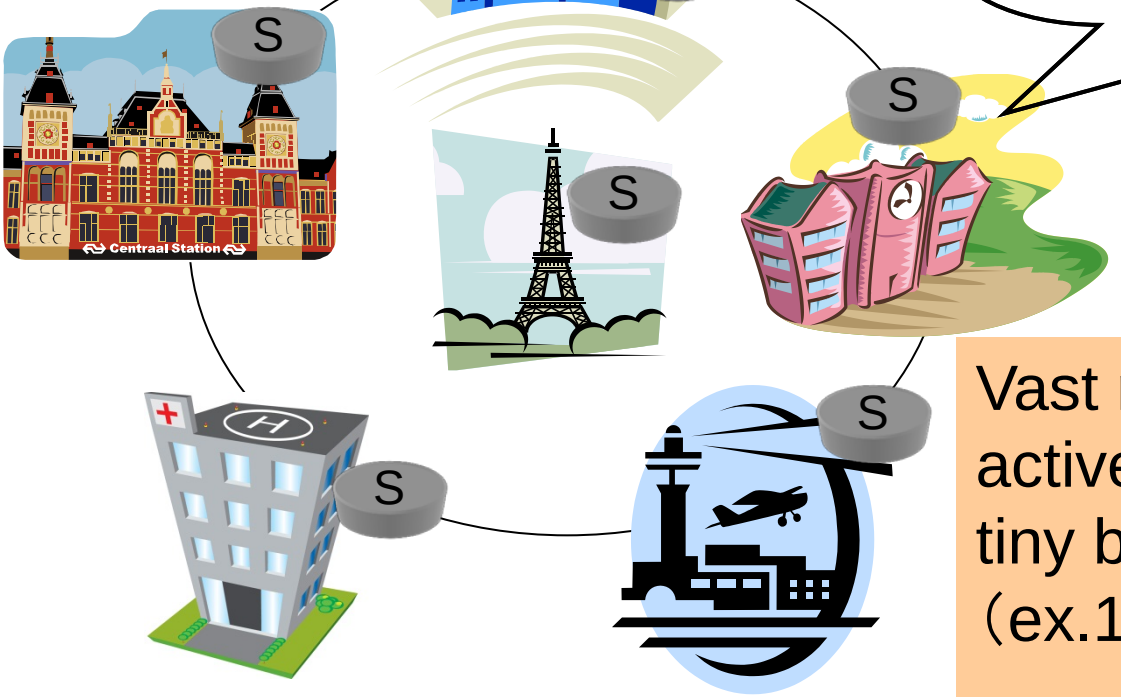
～13B$ market in 2015 (Japan Only)

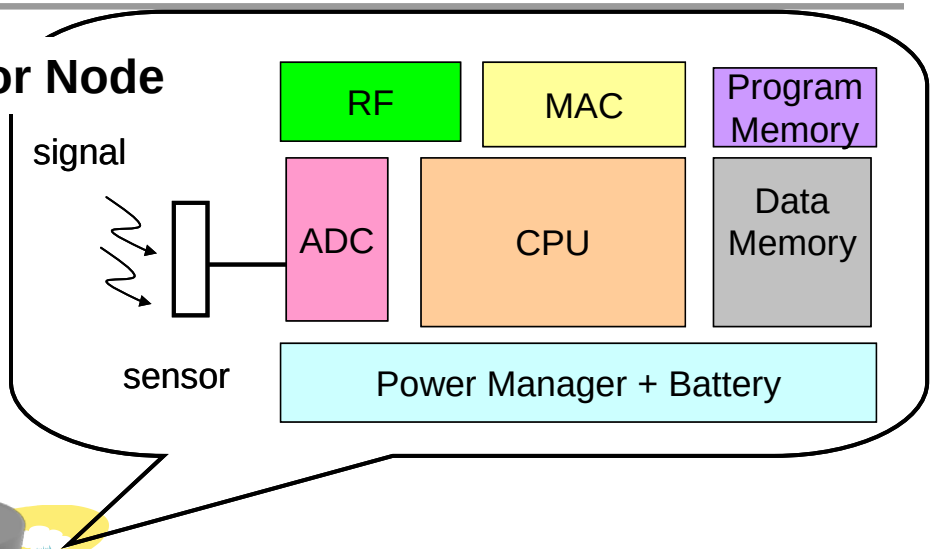


Nikkei Electronics 2009 December 28

Sensor Network and Sensor Node

Sensor network for Social Security and Information Grid





Vast numbers of sensors, active for several years with a tiny battery or a solar cell
（ex.10mW level、100kbps
10m Wireless Network）

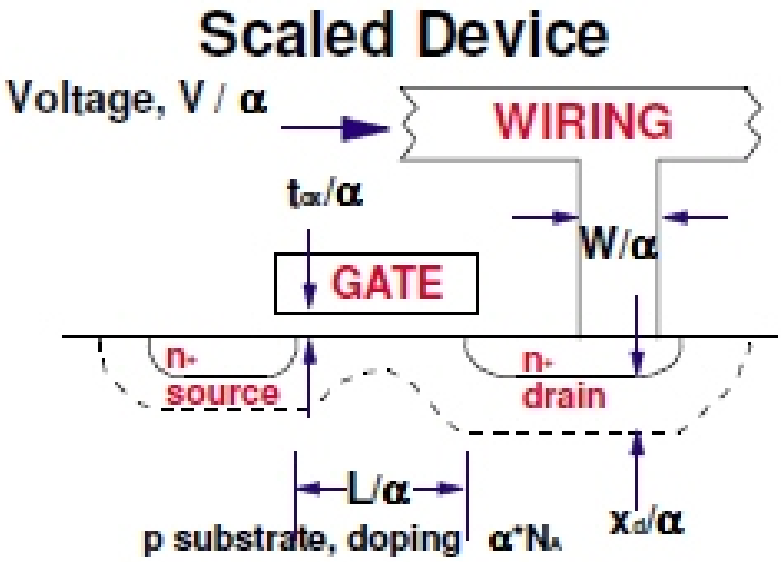
Issues for Sensor Nodes

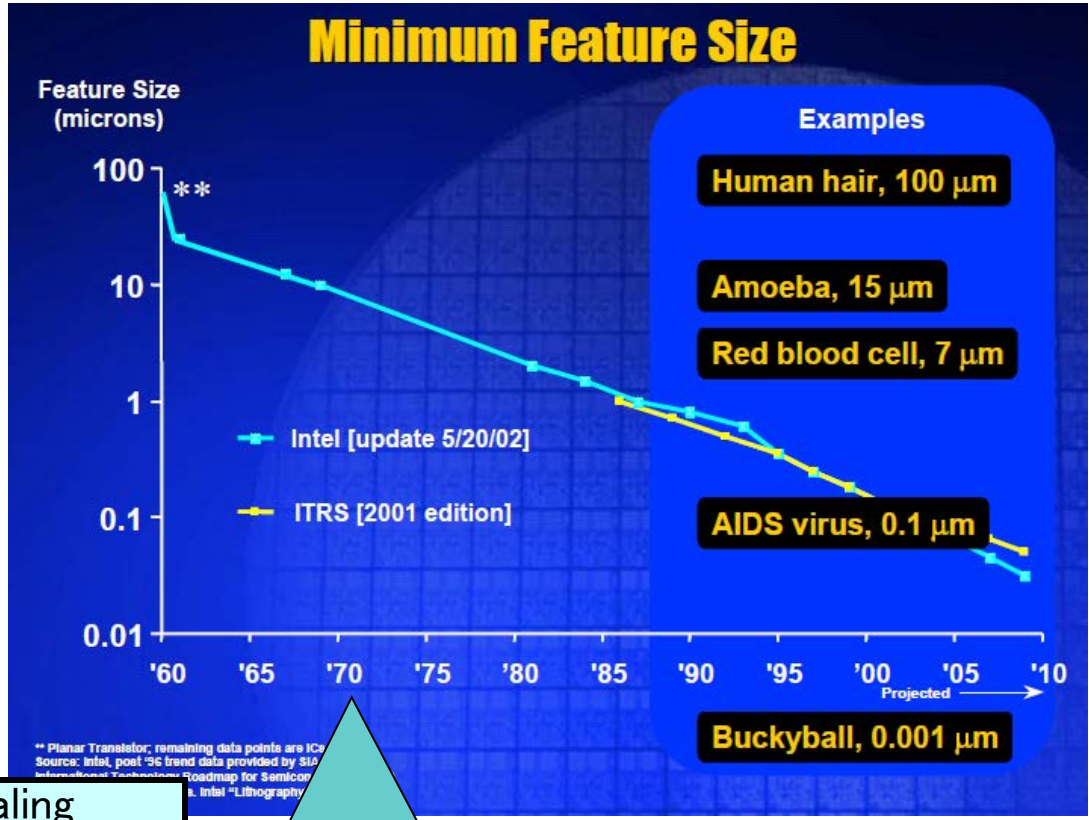
- **Power Saving - Low power , long battery life**
- **Data processing speed – high speed processing with very low power and limited memory capacity**

Basic requirement

- **Large band width – high speed network**
- **Cost - smaller and cheaper !**
- **Flexibility with universal protocol**
- **Information security – Certification between nodes**

Dennard's Scaling Law



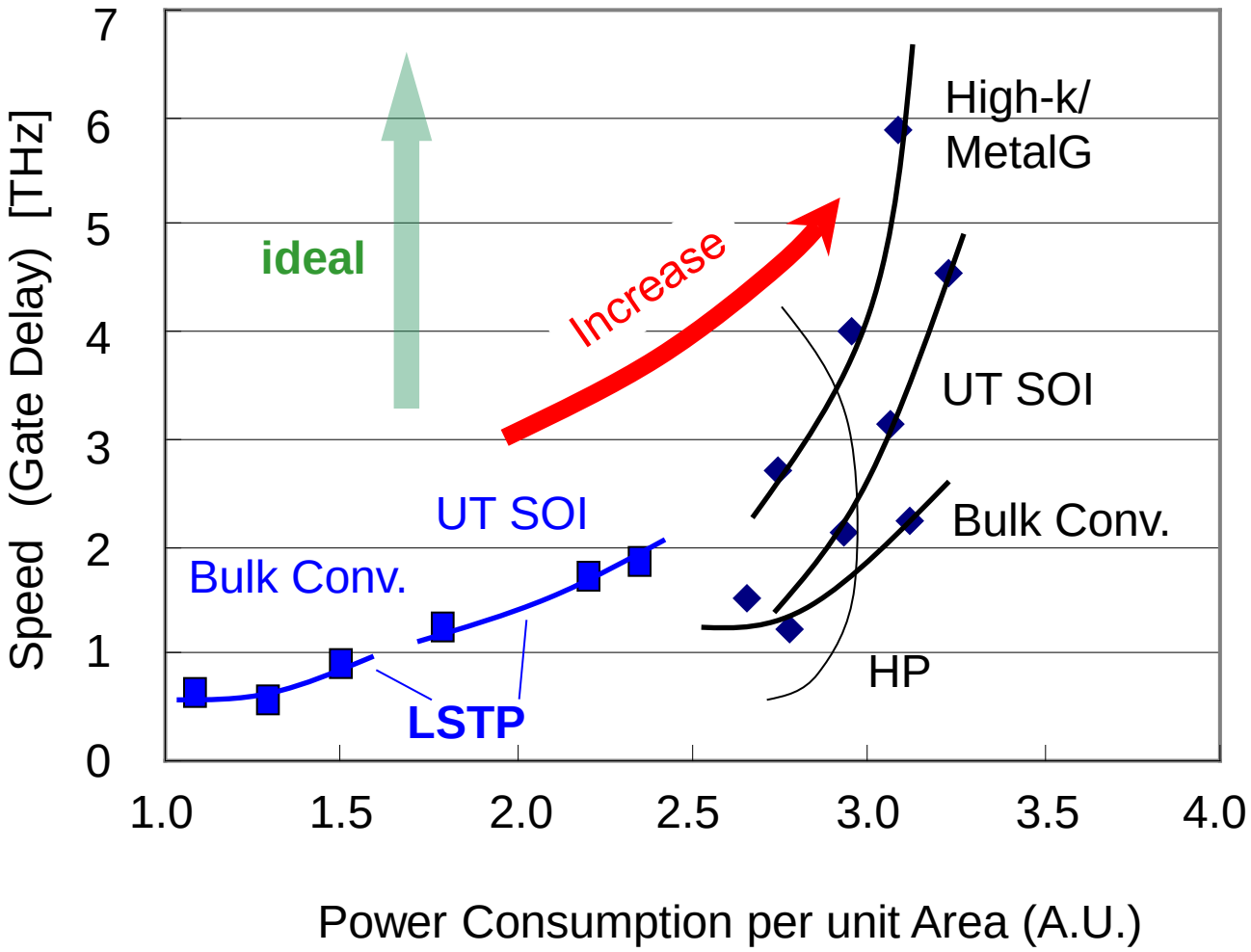


パラメータ	記号	Scaling
Electric Field	$E \propto V/x$	1
Tr density	$1/WL$	K^2
Current	$I \propto WV^2/(LT_{ox})$	$1/K$
Capacitance	$C_{load} \propto LW/T_{ox}$	$1/K$
Speed	$\tau \propto C_{load}*V/I$	$1/K$
Power density	$P \propto VI/LW$	1

Source: Intel (http://www.intel.com), from presentation at ISSCC 2003

High speed processing and low power consumption was satisfied by scaling at the same time.

ITRS device trend: Device Speed vs Power Consumption



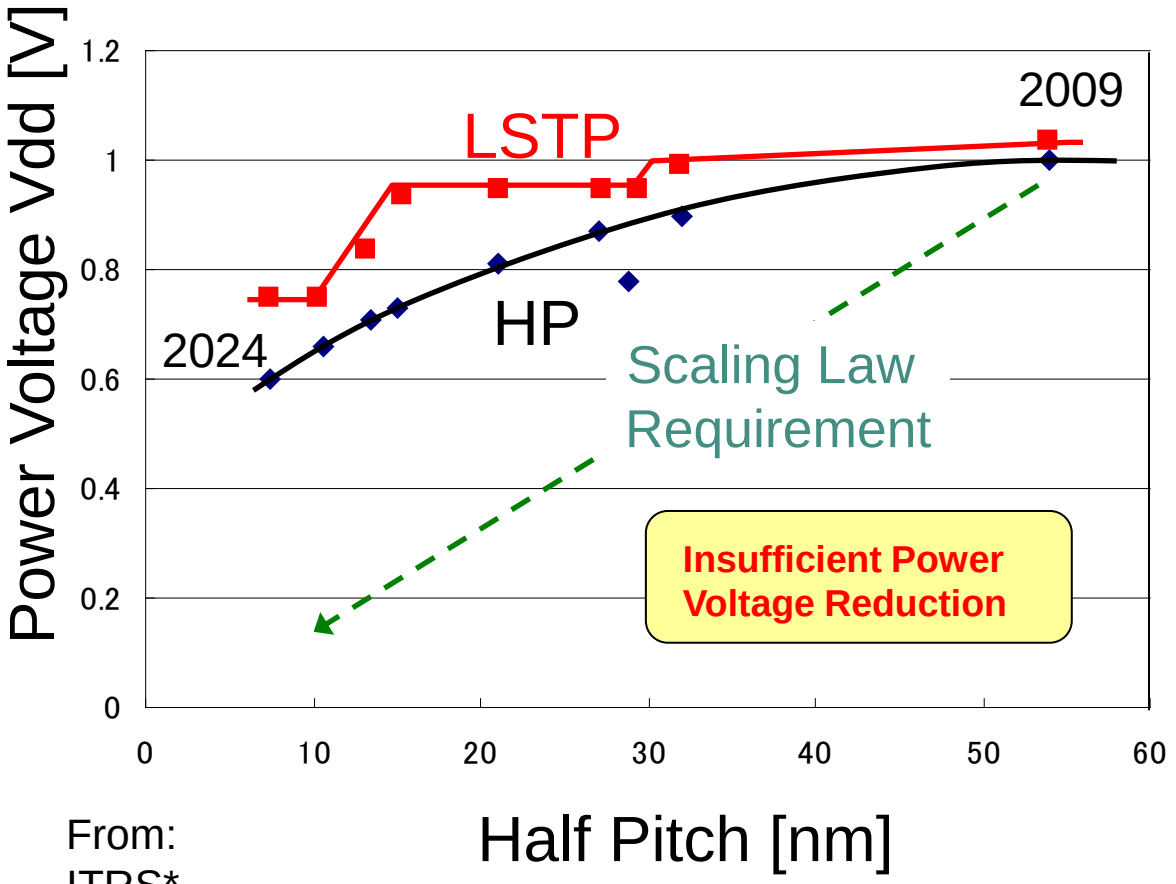
From:
ITRS*
Roadmap 2009

(2009- 2024 trend)

Ideal situation is not expected for further scaling !

Why??

Power Voltage Trend Forecast in ITRS

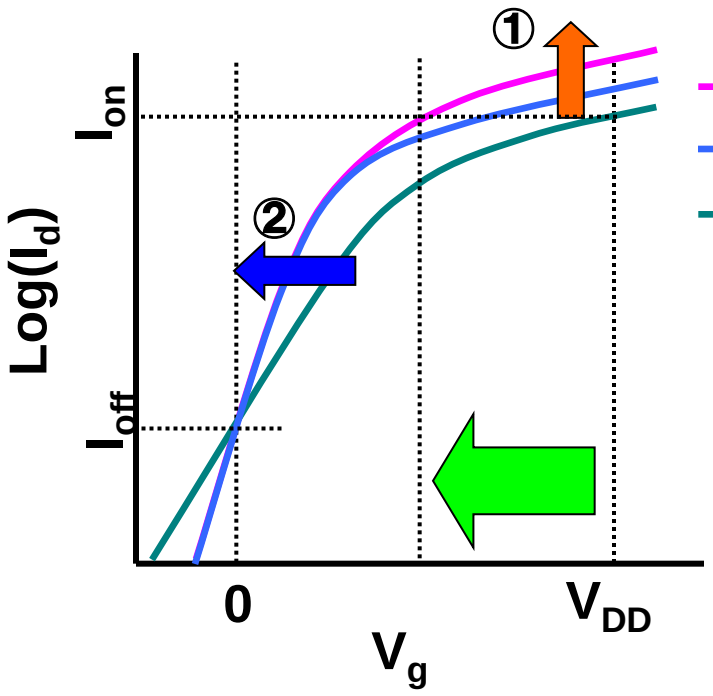


From:
ITRS*
Roadmap 2009

Major Barriers for Power Voltage Reduction

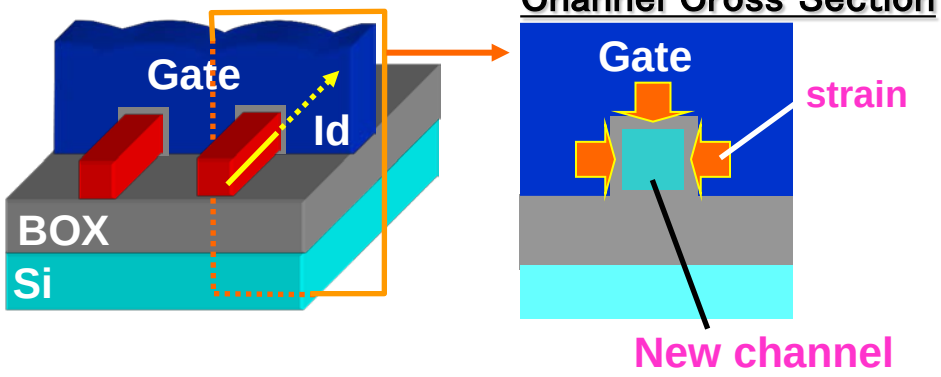
- **Small Ion (Device Speed Degradation)**
- **Off Leakage Current Ioff Increase (Standby Power Consumption Increase)**
- **Relative Threshold Voltage Fluctuation Increase**

Approach: Non-planer structure + Ion Booster



Multi-gate + Ion Booster
Multi-gate
Bulk Planer

Multi-Gate



① Large Id ⇒ Stress engineering ,
High-mobility channel material

② Steep subthreshold ⇒Multi-gate

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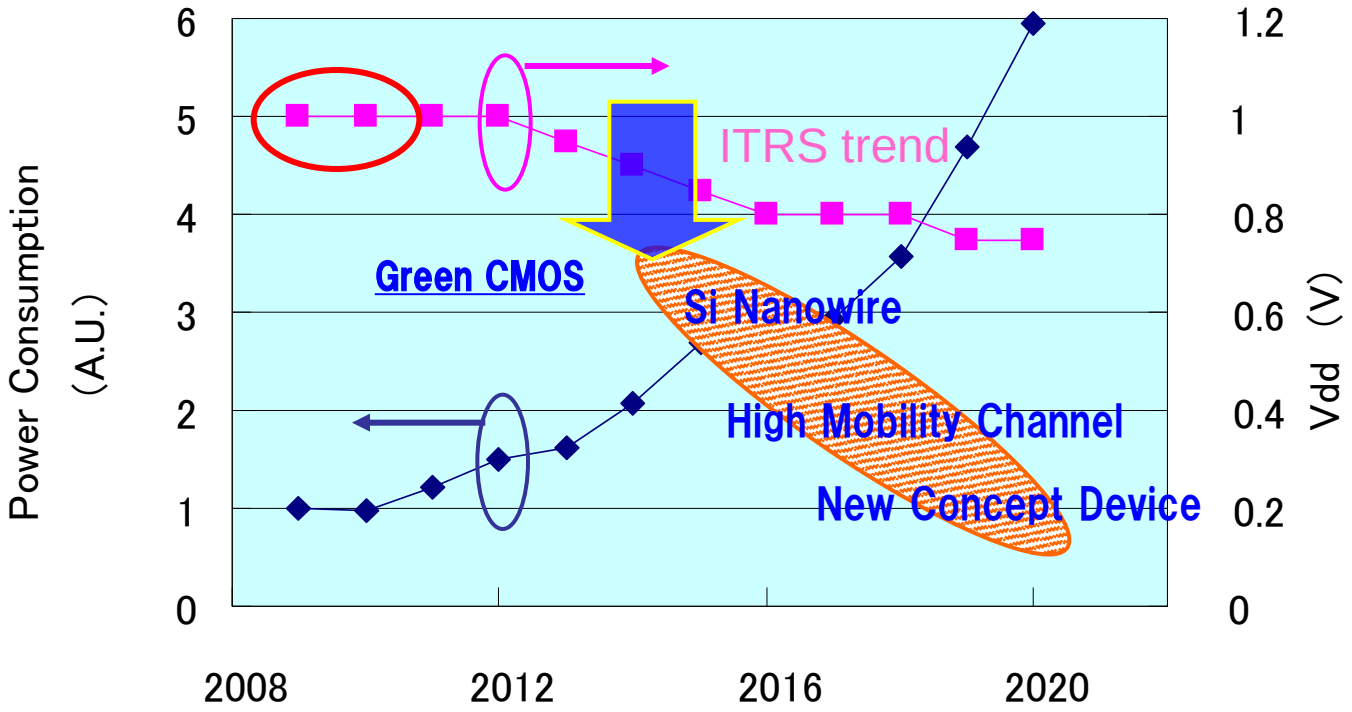
Low power consumption CMOS Development



$$\text{Power} = \alpha \cdot f \cdot C_{load} \cdot V_{dd}^{2} \cdot n + I_{off} \cdot V_{dd} \cdot n$$

Active power　　Standby Power

α: Activation Ratio, f: Clock Freq., C_{load}:Load Capacitance,

V_{dd}:Supply Voltage, I_{off}, n: Amount of devices

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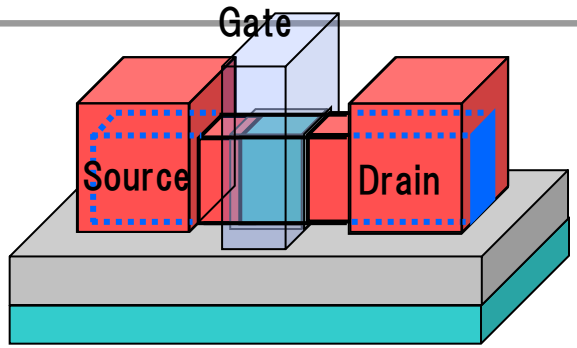
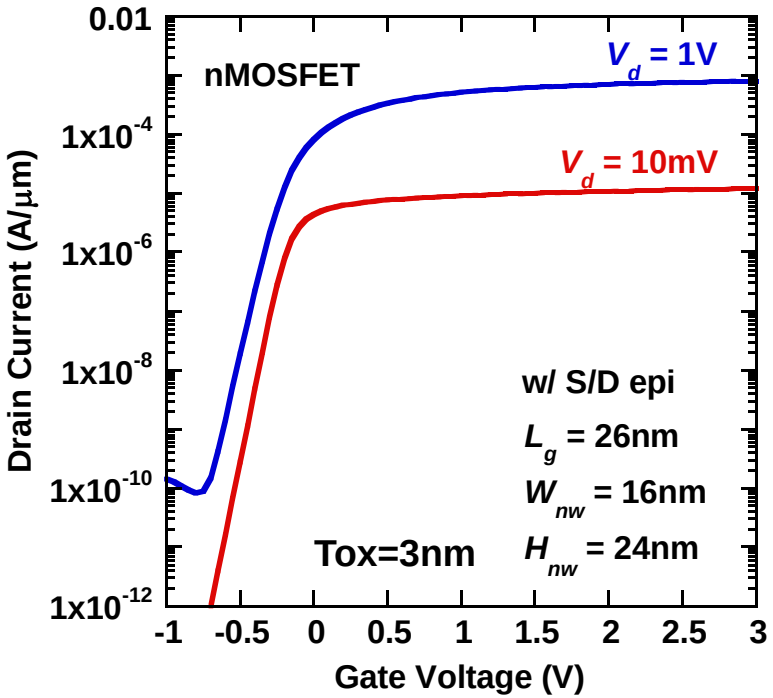
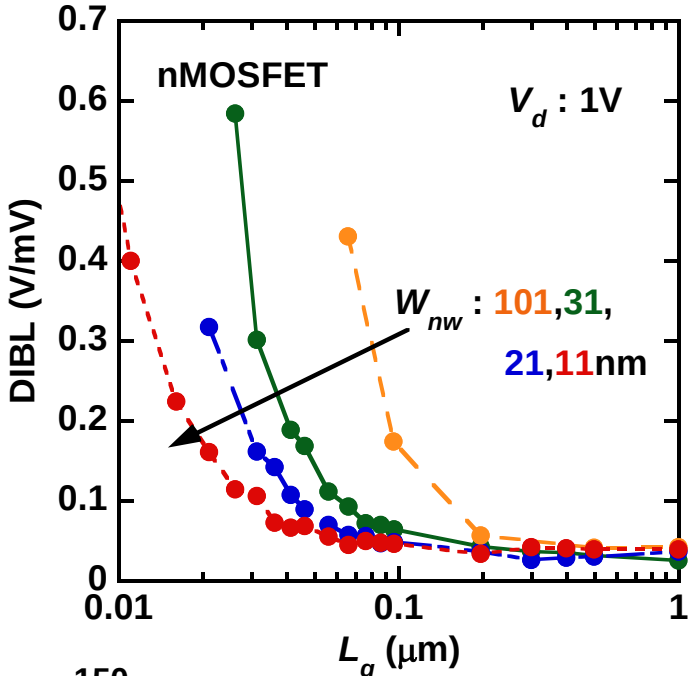
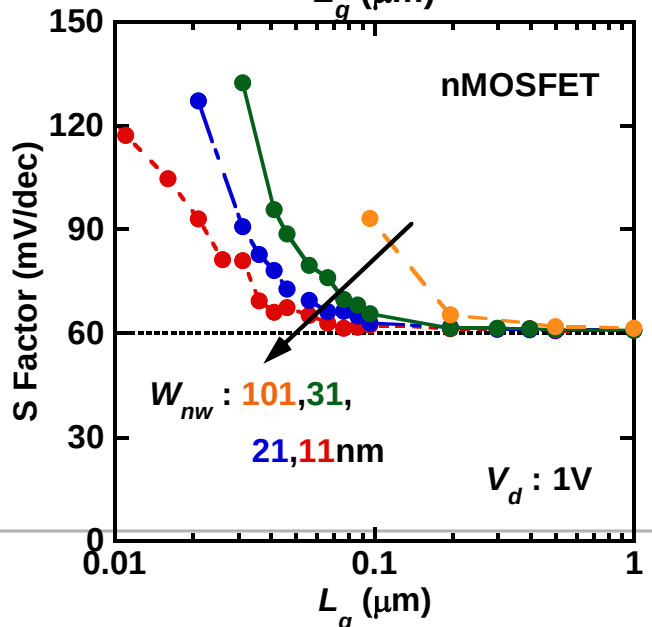
Si NW: Short Channel Effect Suppression





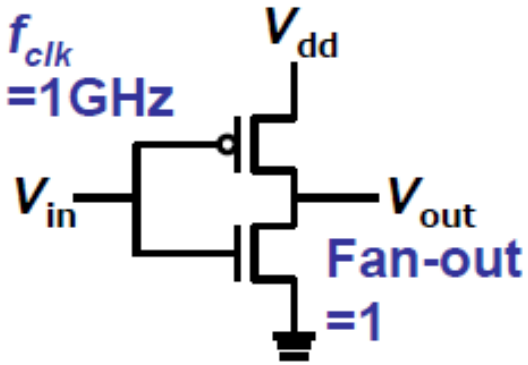


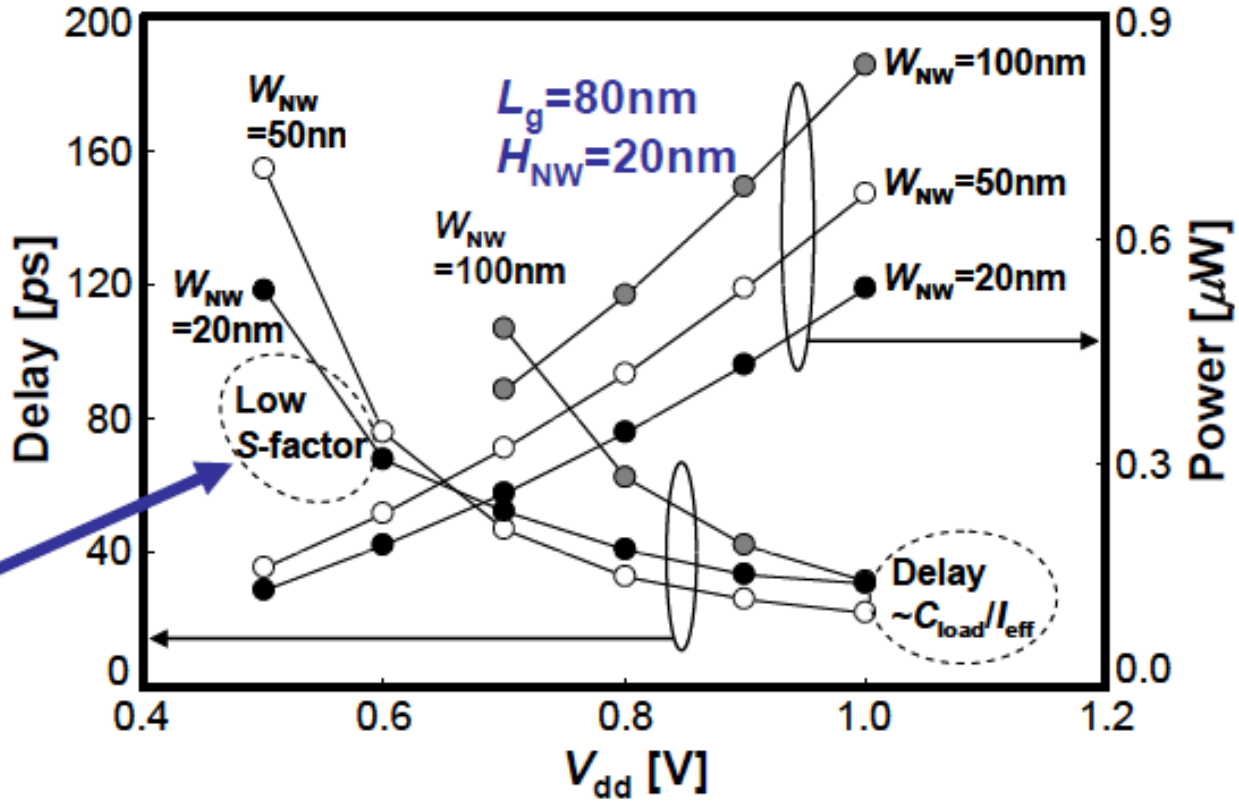


Wire width reduction leads to steeper subthreshold swing

Inverter Performance: Delay and Power

(Simulation)





Delay is suppressed in thin NW Tr.

In the low V_{dd} operation, the sub-threshold characteristic is a key in the circuit performance.

⇒Further NW thinning is desired

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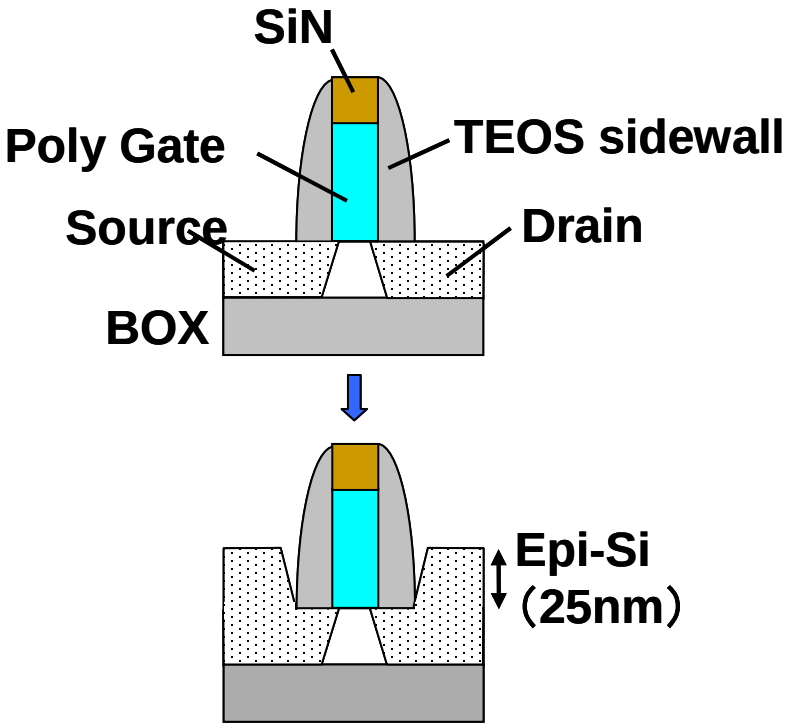
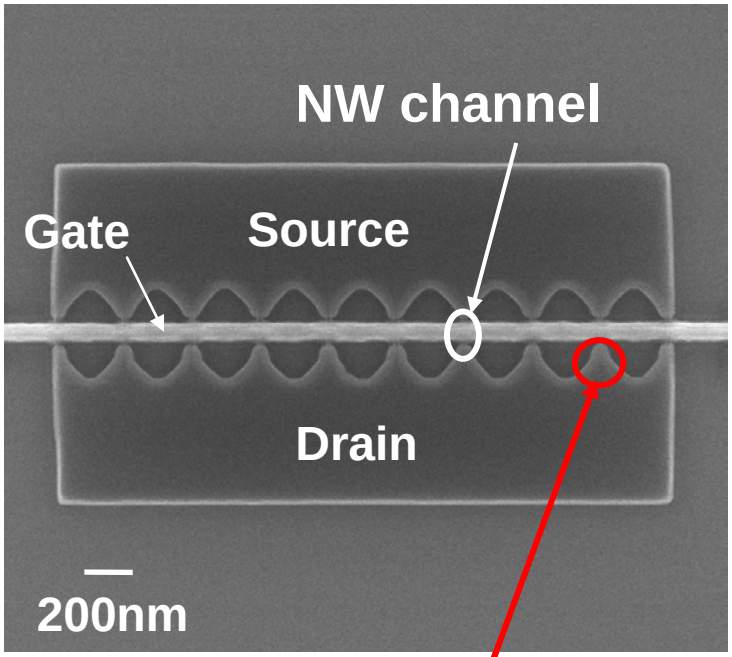
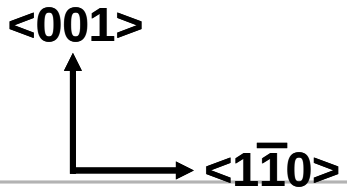
Si NW: Parasitic Resistance Reduction

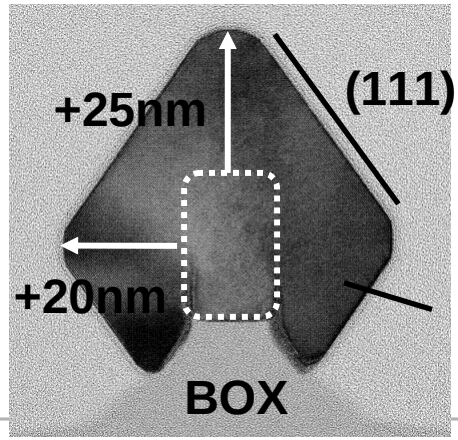




Enlarged by Epi-growth

Cross sectional View of NW after Epi growth on S/D





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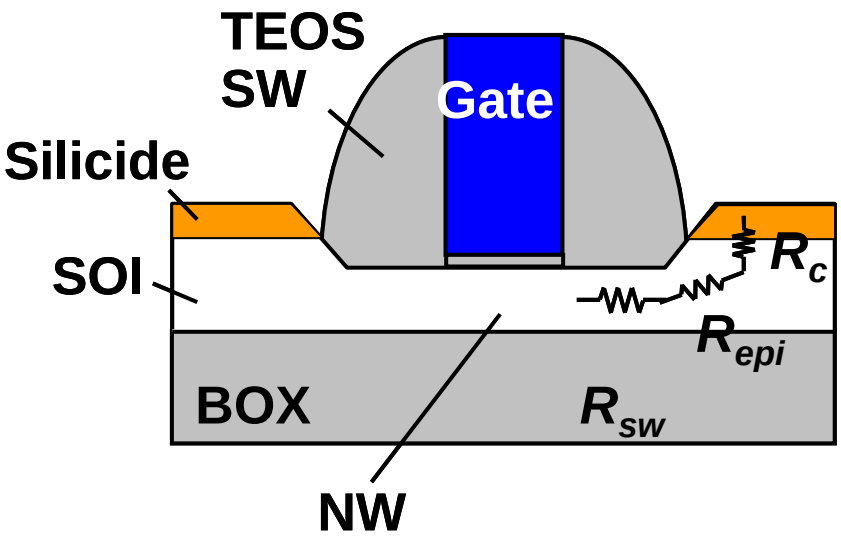
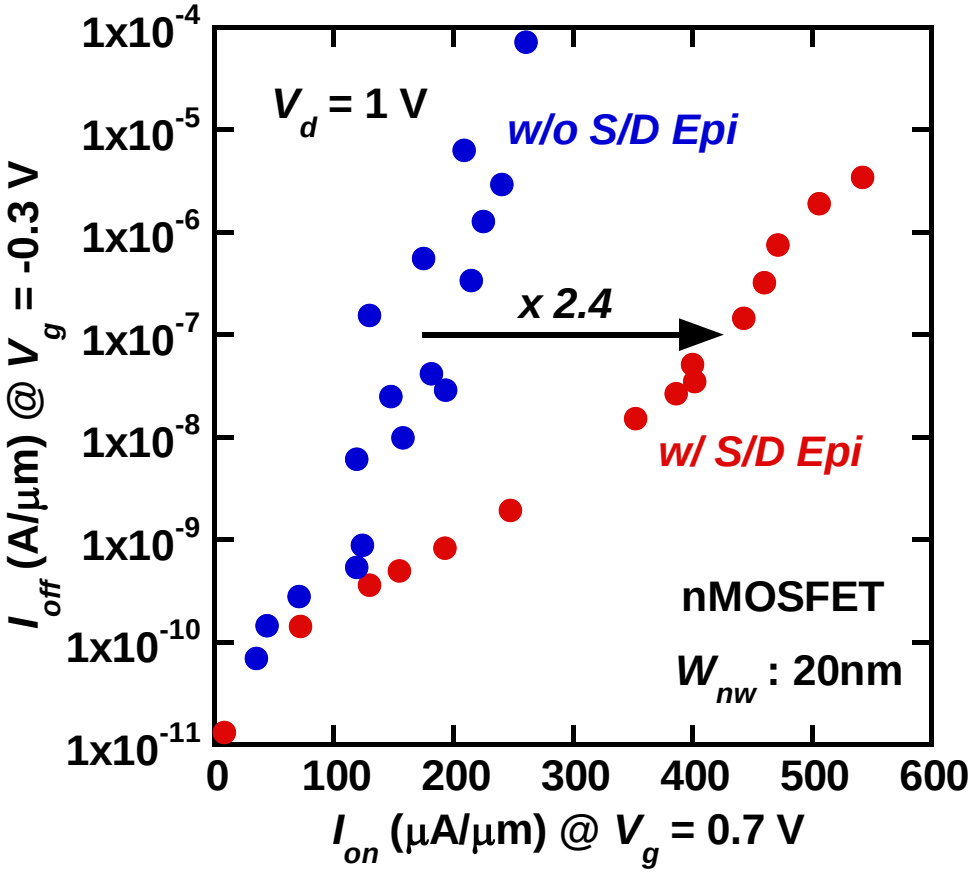
NW: Parasitic Resistance Reduction





Ion increase by a factor of 2.4 was obtained.
⇒Parasitic resistance reduction is important especially for NW transistors.

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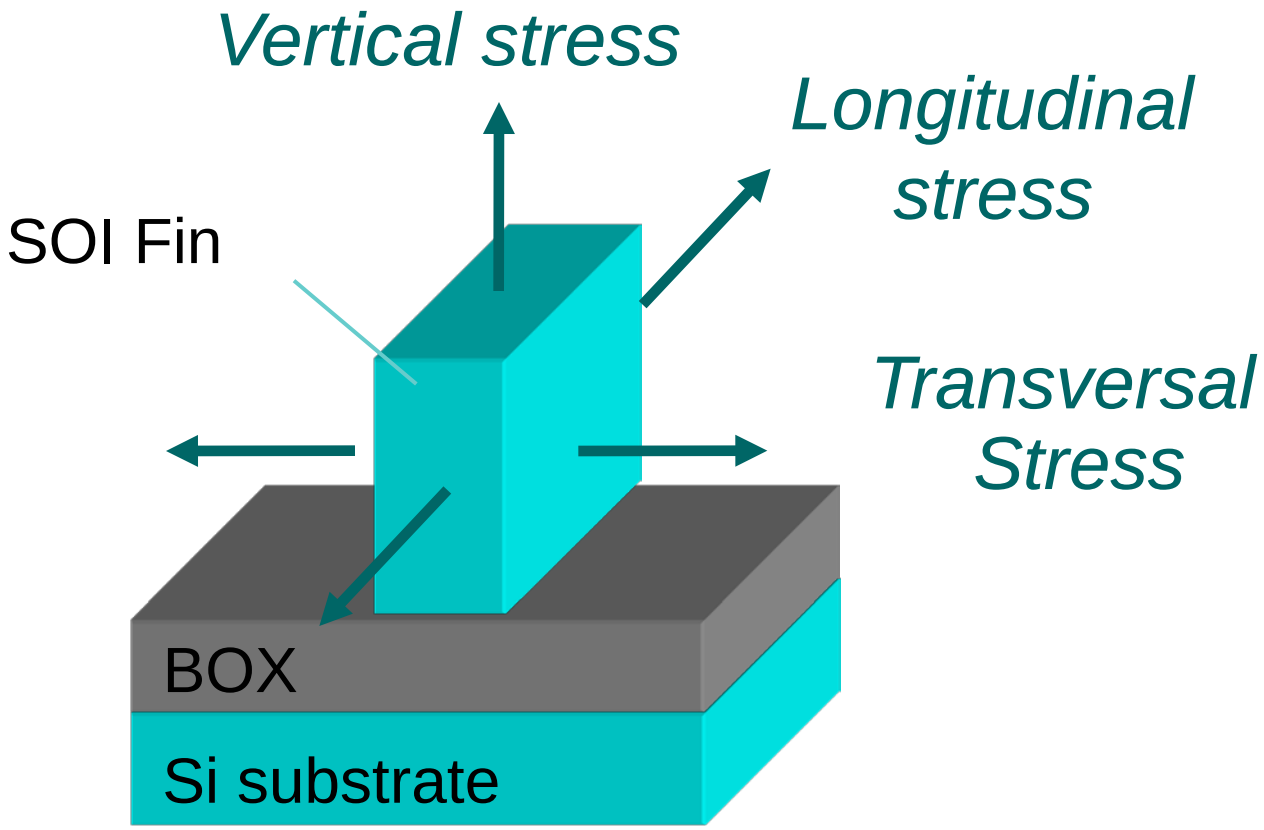
3D stress engineering for NW MOSFETs



- **In addition to longitudinal stress, transversal and vertical stress is effective for NW MOSFETs**

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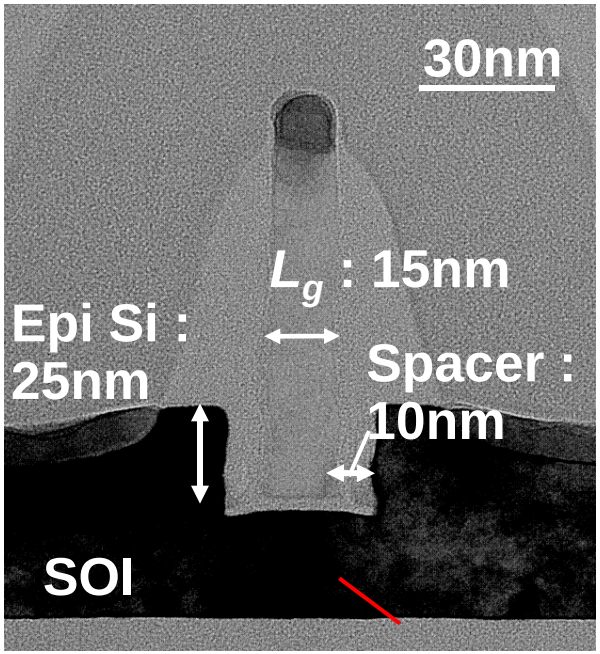
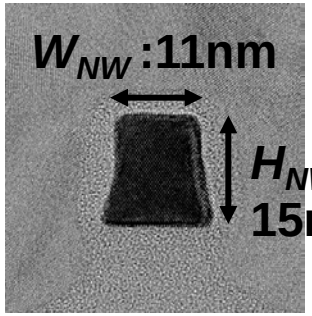
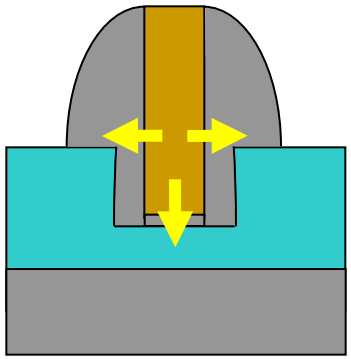
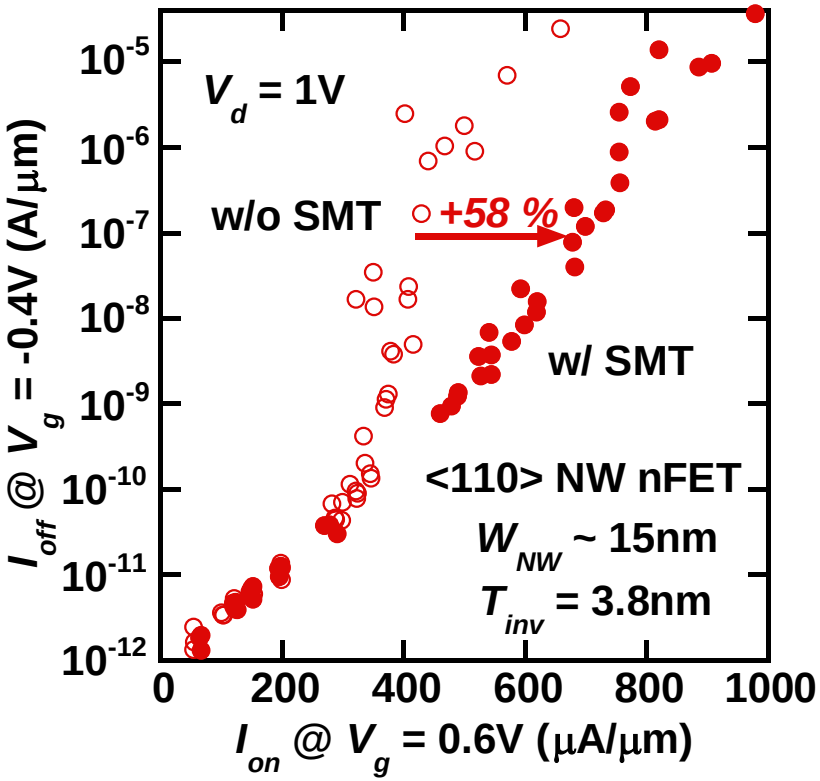
Si Nanowire Transistors: Stain Technique





Stress Memorization Technique (SMT) of Poly-Si Gate





Stress engineering to nanowire channel is highly effective for the performance improvement of nanowire transistors.

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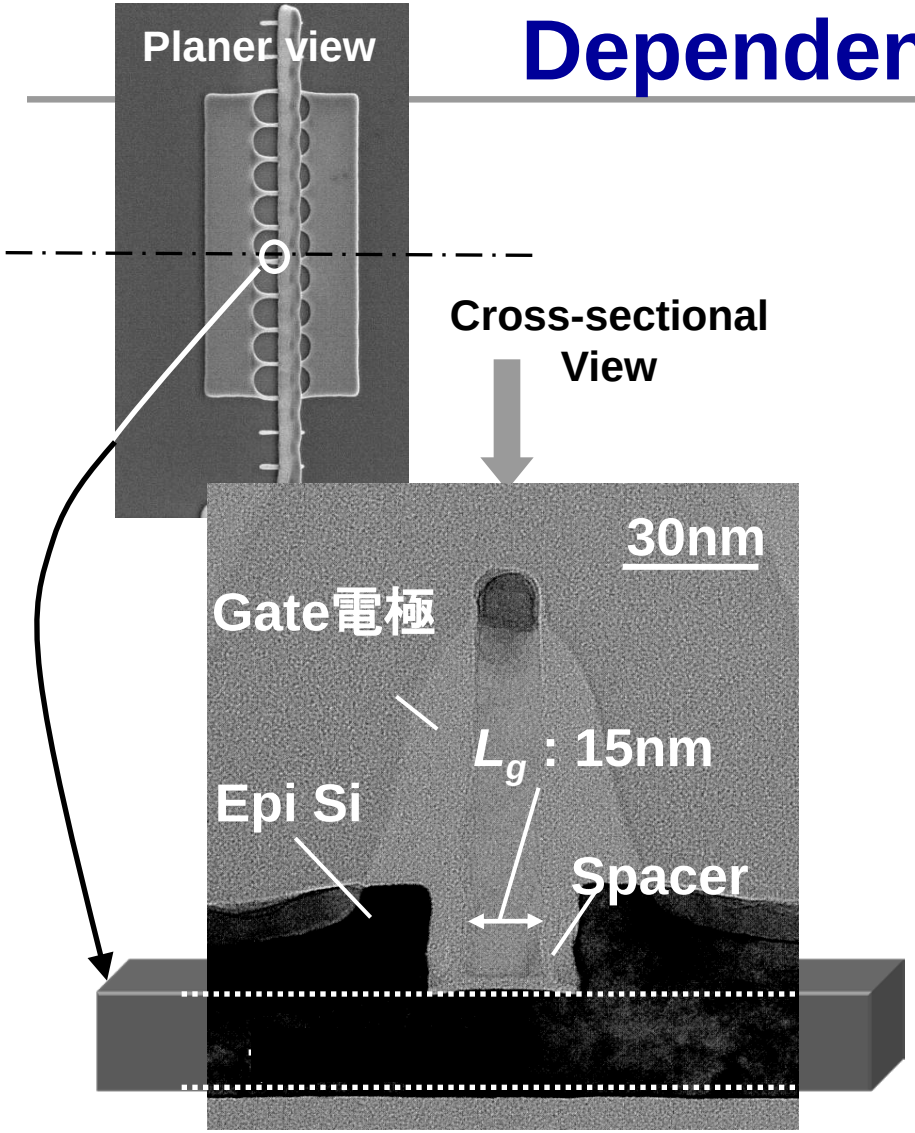
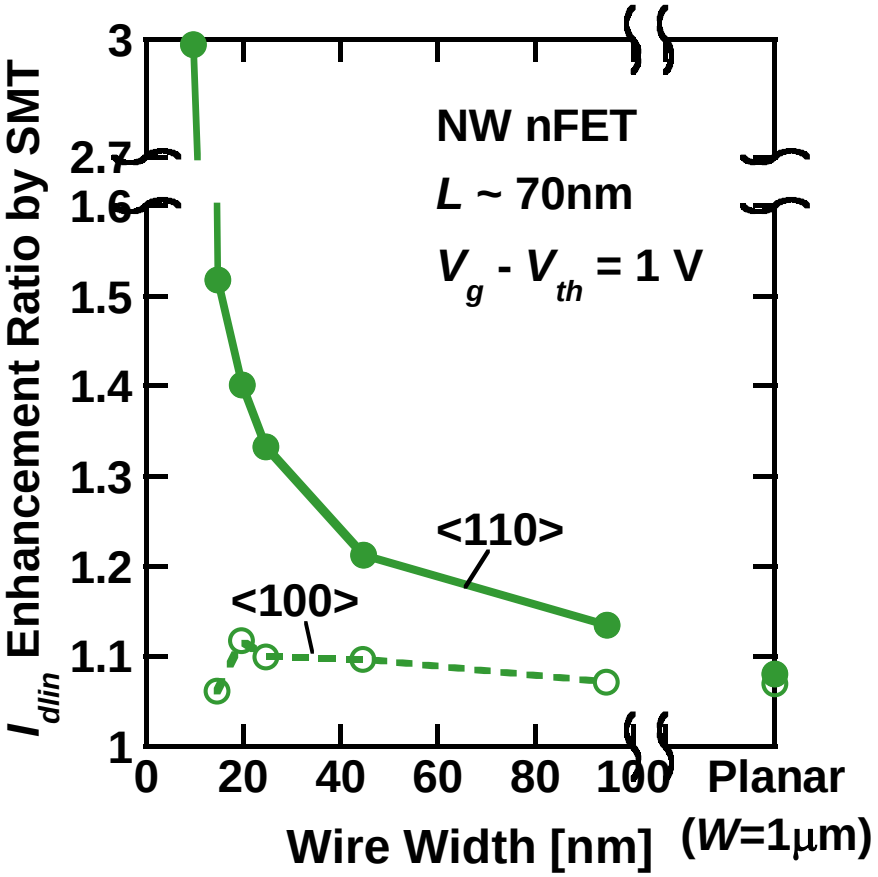
Dependence on wire width





Strain is especially effective for thinner NW.

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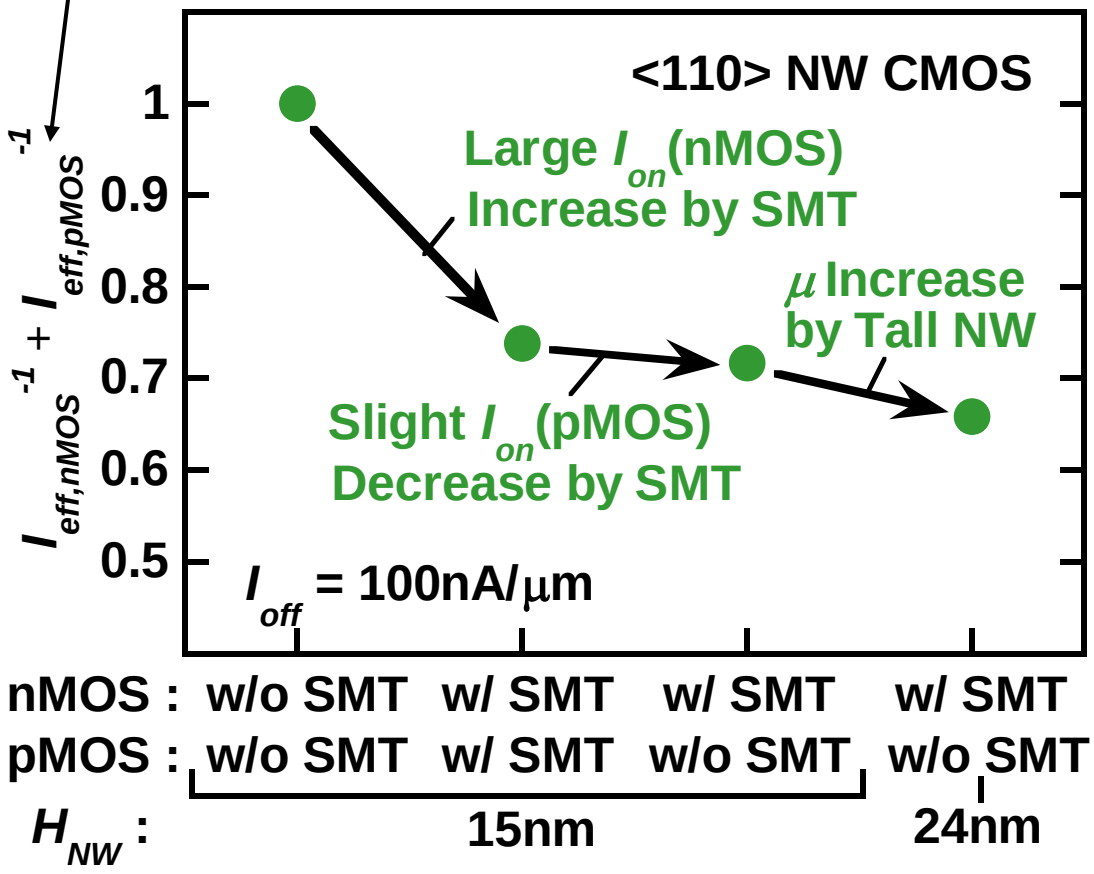
Performance of SMT NW CMOS

I_{eff}^{-1} : Measure of CMOS inverter delay



CMOS performance is greatly improved by NW .

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High-mobility channels for CMOS

Material	Strain	Normalized mobility (vs. unstrained Si)		Remarks
		n	*p*	
Si	biaxial	2 [1]	1.4 [1]	
	uniaxial	1.7 [2]	3 - 4 [2, 10]	
$Si_{1-x}Ge_x$	biaxial		2.3 [3] 6~10 [4]	x=0.42 x=0.92
Ge	No	1.4 [5] 3 [7]	2 [6]	with high-k theory
	Uniaxial biaxial	4.1 [7]	 10~20 [8,9]	theory buried channel
GaAs	No	6.3 [2]	[illegible]	Low field/bulk
InAs	No	13-20 [2]	0.2-0.9 [2]	Low field/bulk

pFET

p&nFET

nFET

[1] K.Rim et al., IEDM 2003, [2] S. E. Thompson, IEDM 2006, [3] T.Tezuka et al., IEDM 2001, [4] T.Tezuka et al., 2004 Symp. on VLSI Tech. [5] H. Shang et al., IEDM 2002, [6] C. Chui et al.,IEDM 2002, [7] Y.-J. Yang et al., APL **91**,102103 (2007).[8] M. L. Lee et al., IEDM 2003, [9] T. Irisawa et al., APL **81**, 847 (2002). [10] S. Mayuzumi et al., 2009 Symp. on VLSI Tech.

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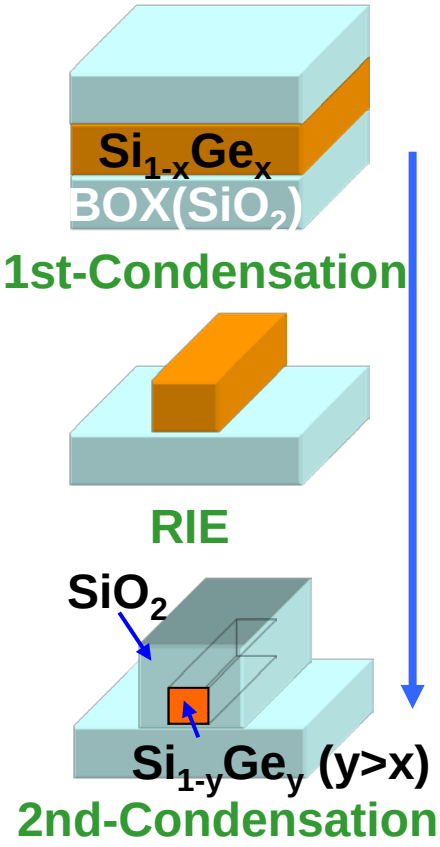
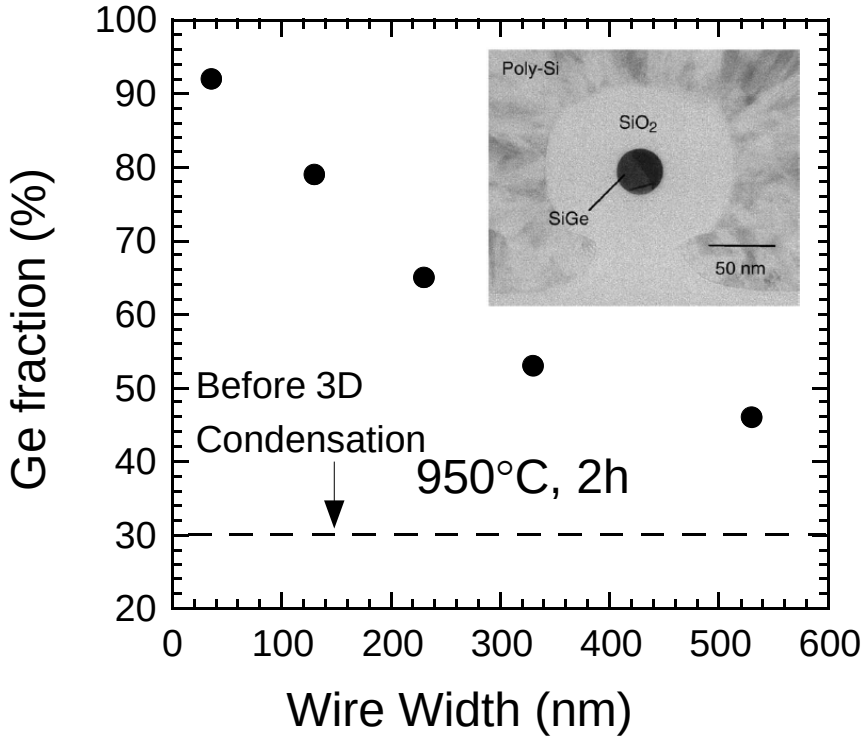
SiGe Nano Wire formed by Ge condensation process





- ✓ **Higher Ge fractions for the narrower mesas**
- ✓ **Formation of Ge-rich and narrow SiGe wires**
- ✓ **Compressive stress is imposed at the same time**

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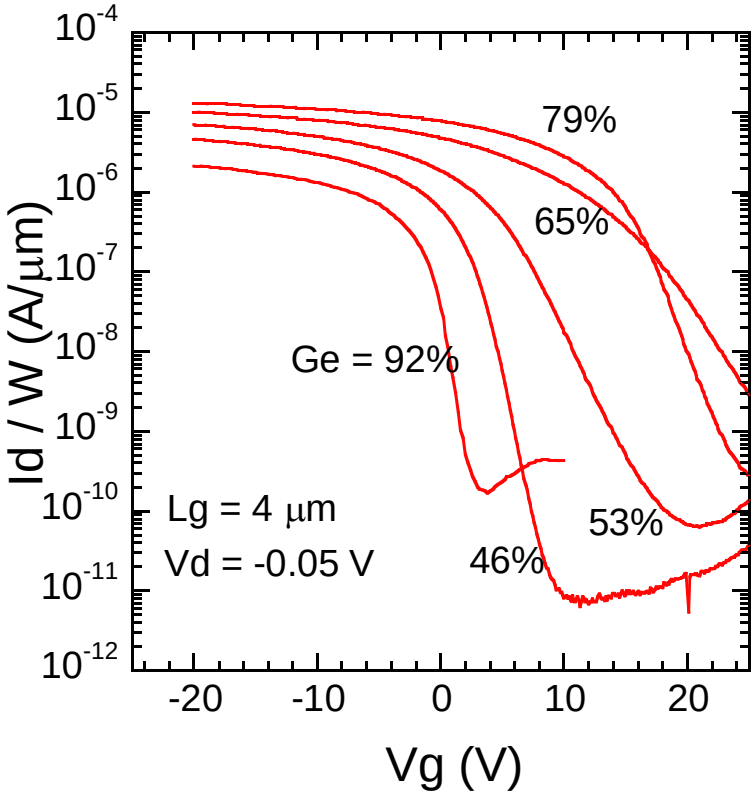
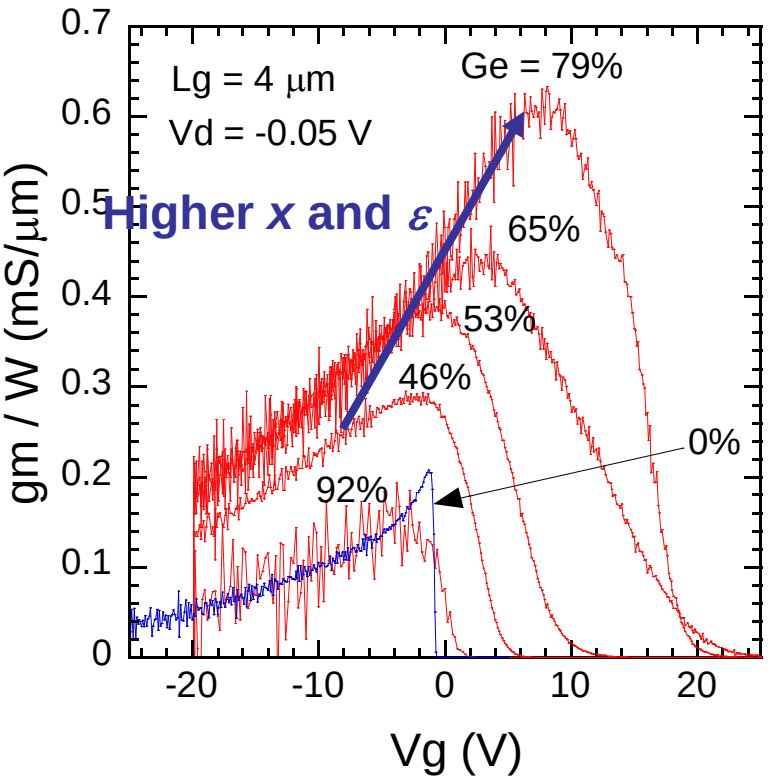
SGOI-wire pFETs





- ✓ **On/off ratio >10^4**
- ✓ **Higher g_m by a factor 3 due to higher Ge fraction, uniaxial compressive strain and {110}-like sidewall**

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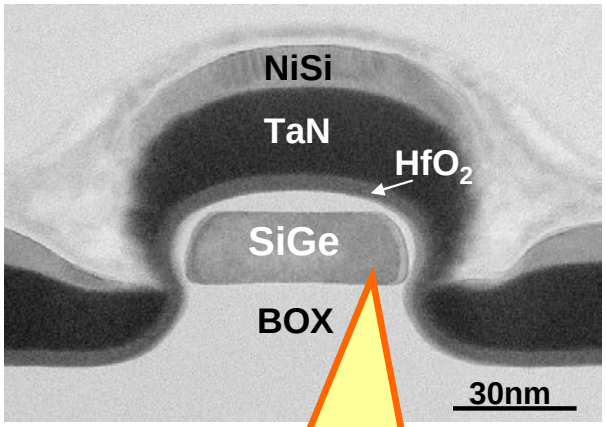
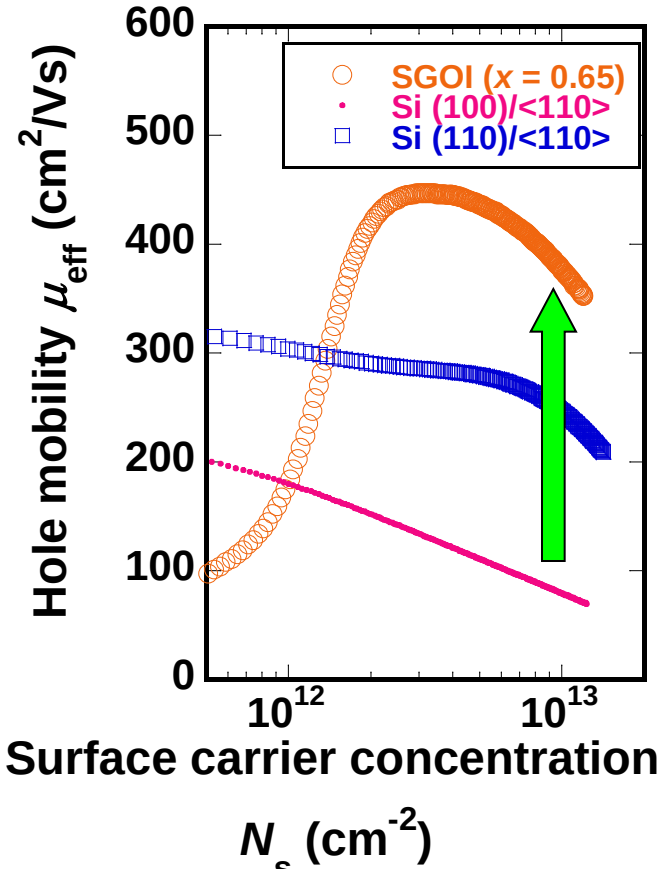
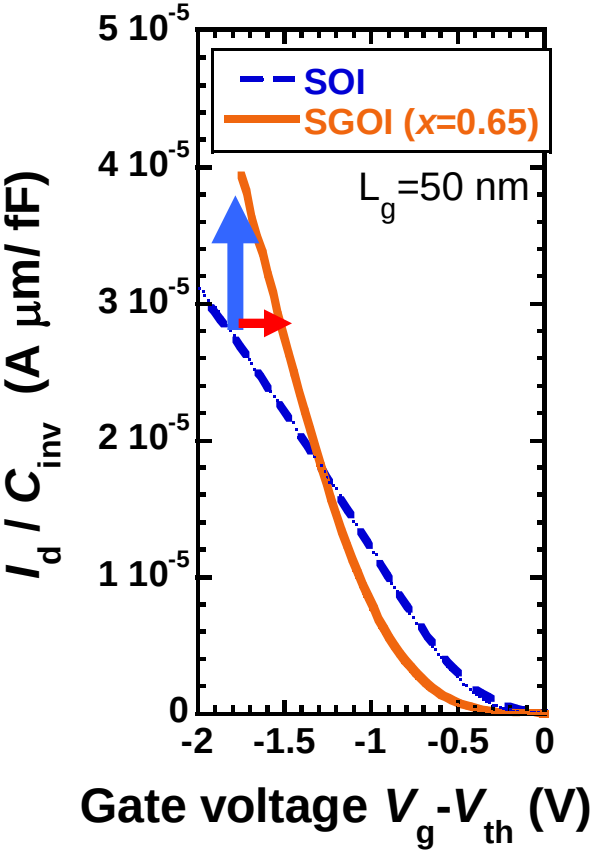
➢ SiGe-Trigate pFET Lg=50nm



x_{Ge}=0.65
Uniaxial strain :2.7%





- Mobility enhancement x4.9
- Id increase 45% (Power reduction 39% by overdrive decrease)

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How about NMOS?

- **Higher electron mobility of Ge than Si**

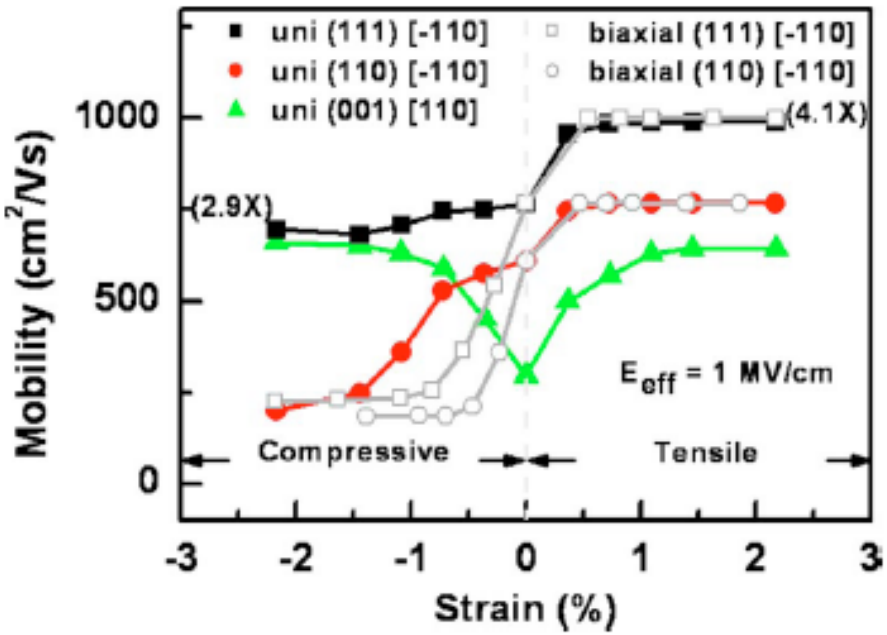
	Si	Ge
μ_e	1500	3900
μ_h	450	1900

- **Tensile strain in Ge … μ_e enhancement**

Tensile strain over 1 %

⇩

4 times higher than unstrained Si



Y.-J. Yang et al., APL **91**,102103 (2007).

Possibility of strained Ge-nMOS in combination with high-speed Ge-*p*MOSFETs

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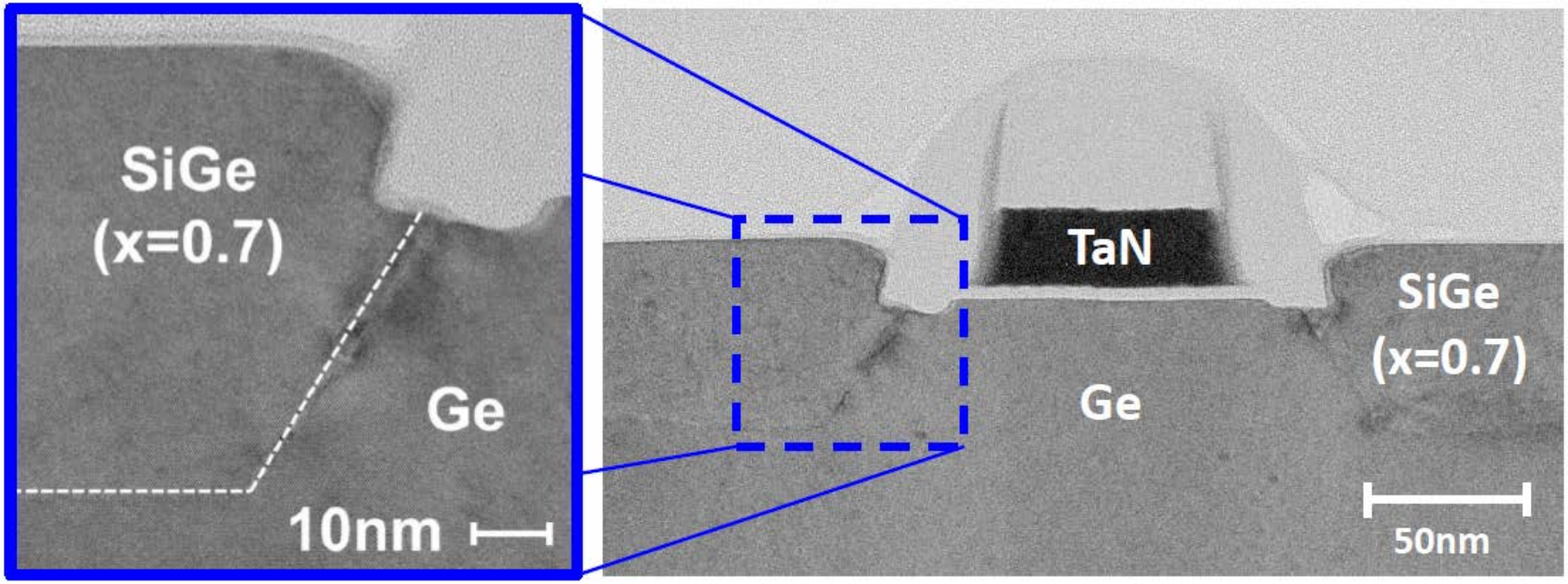
X-TEM image of nMISFET with SiGe S/D



- ✓ Atomically flat surfaces and interfaces between SiGe and Ge
- ✓ Seamless growth under gate edge
- ✓ Some defects near the SiGe/Ge interface

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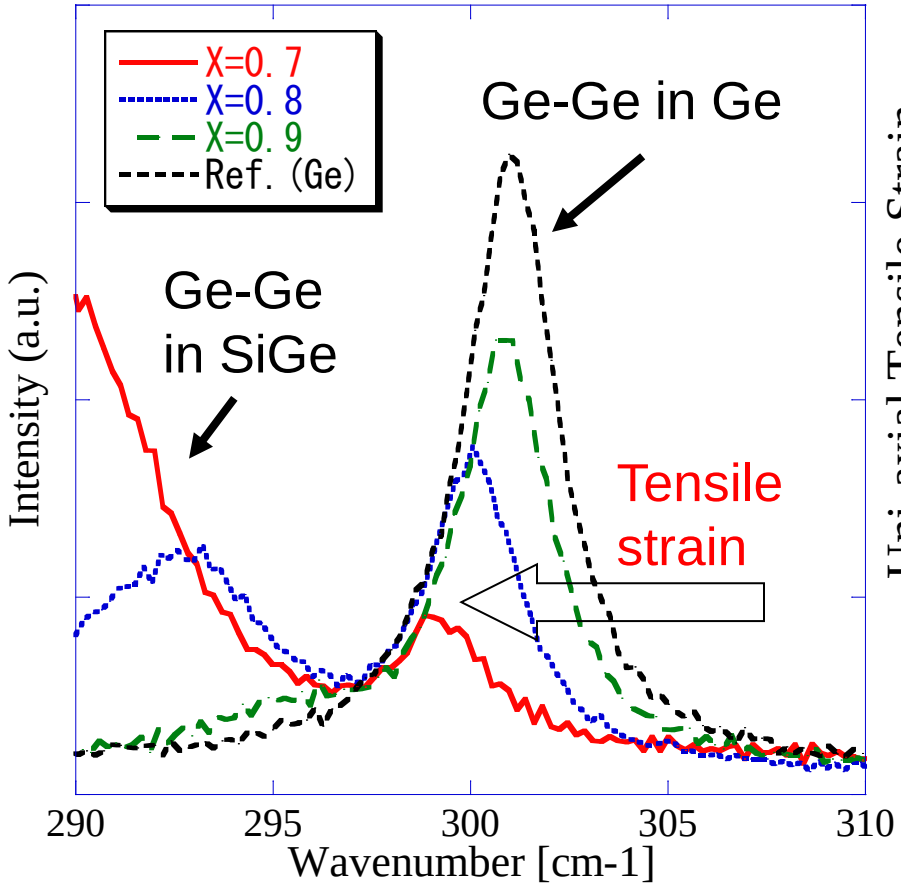
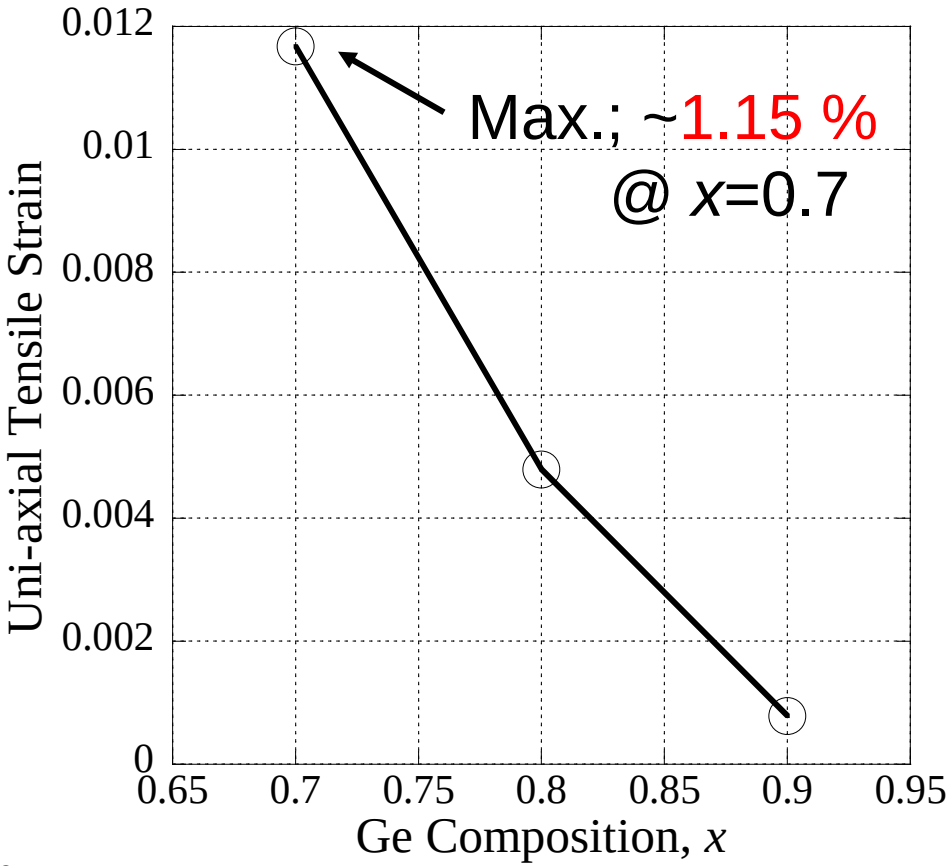
Tensile strain vs Ge comp. of stressors

Raman spectra @ Gate edges





Lattice mismatch between Ge and $Si_{0.3}Ge_{0.7}$ ~1.3%

Tensile uni-axial strain over 1 % was introduced @ x=0.7

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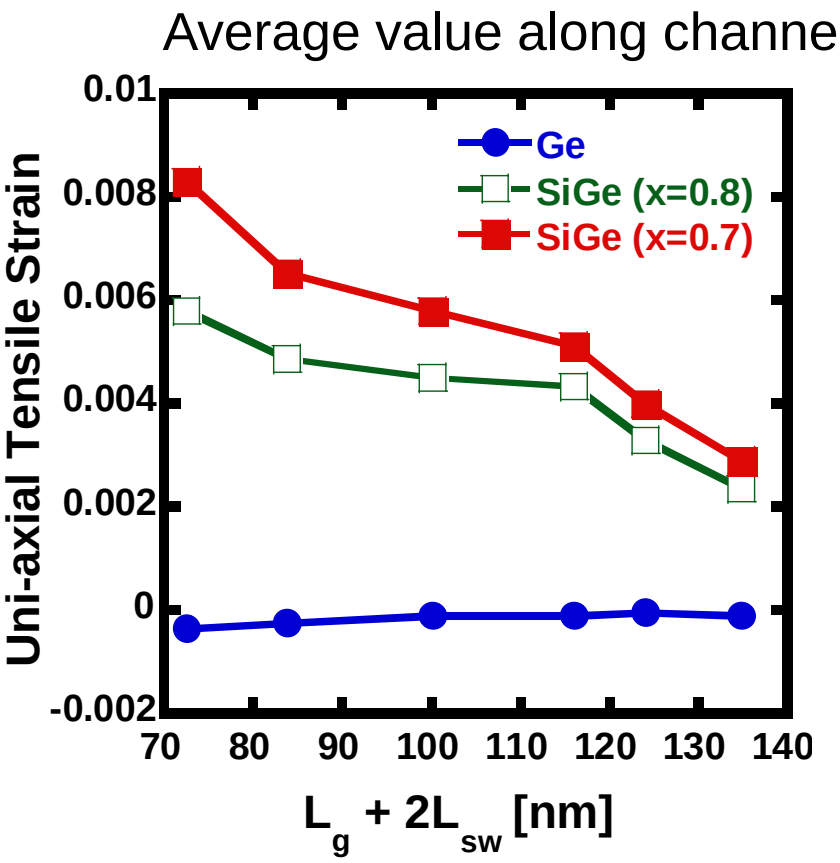
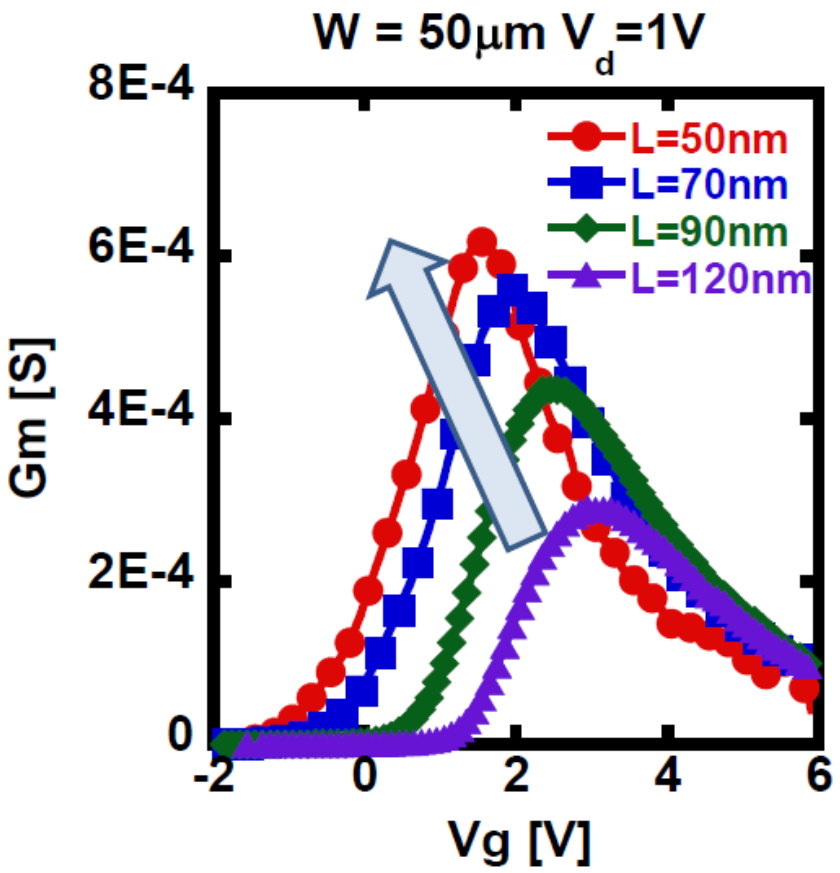
Lg dependence of strain and Gm increase





Gmmax increased by a factor of 2 by Lg scaling

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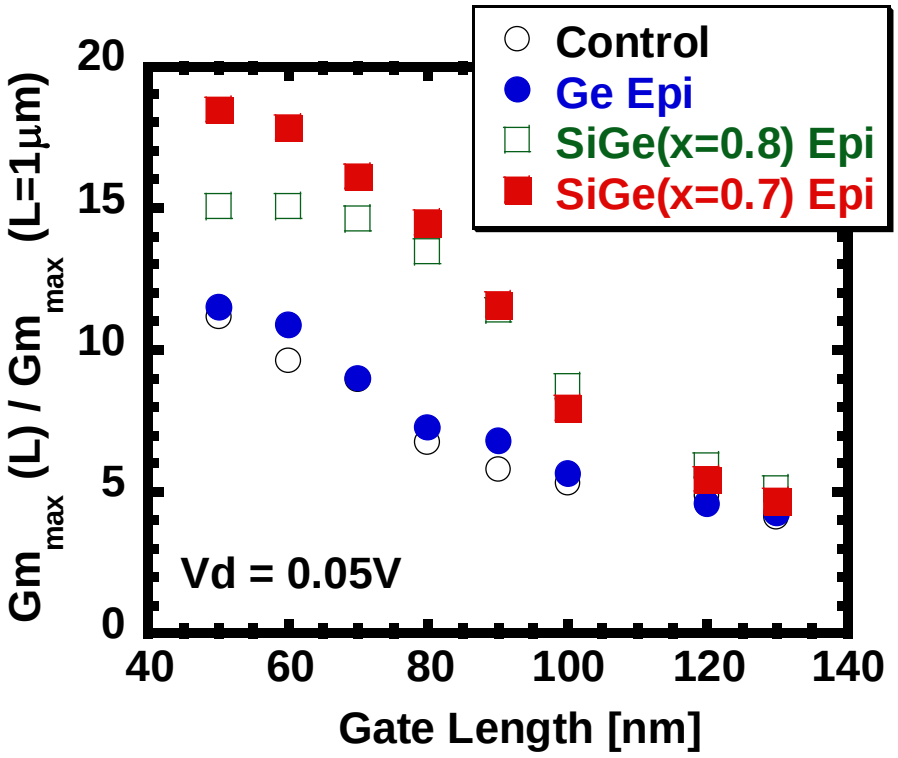
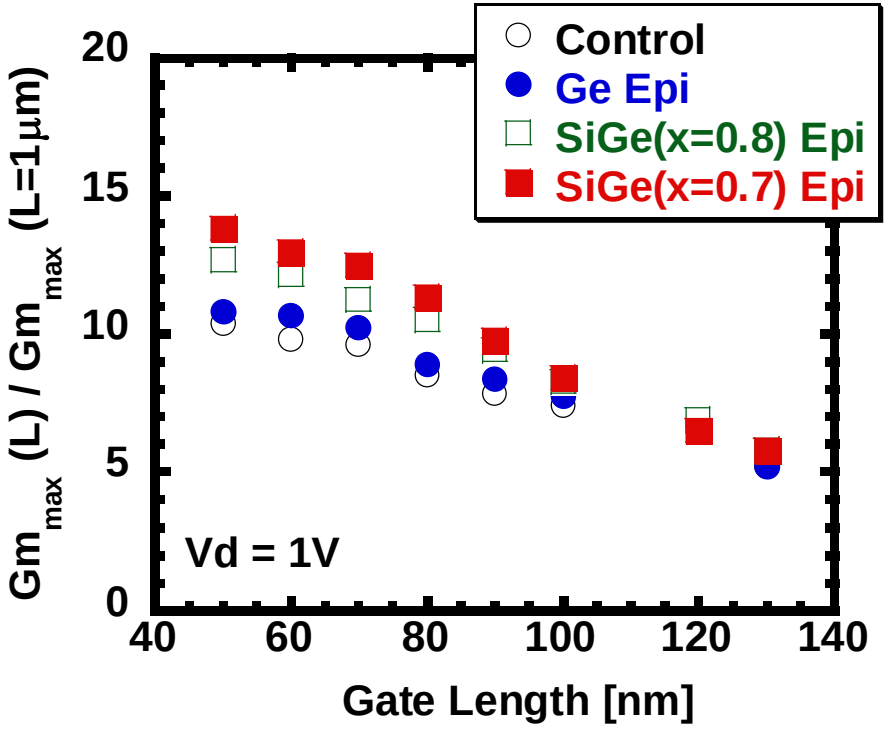
Normalized Gm max gain by 1% strain





About 60% gain for Gmmax at Vd=0.05V

About 30% gain for Gmmax at Vd=1V

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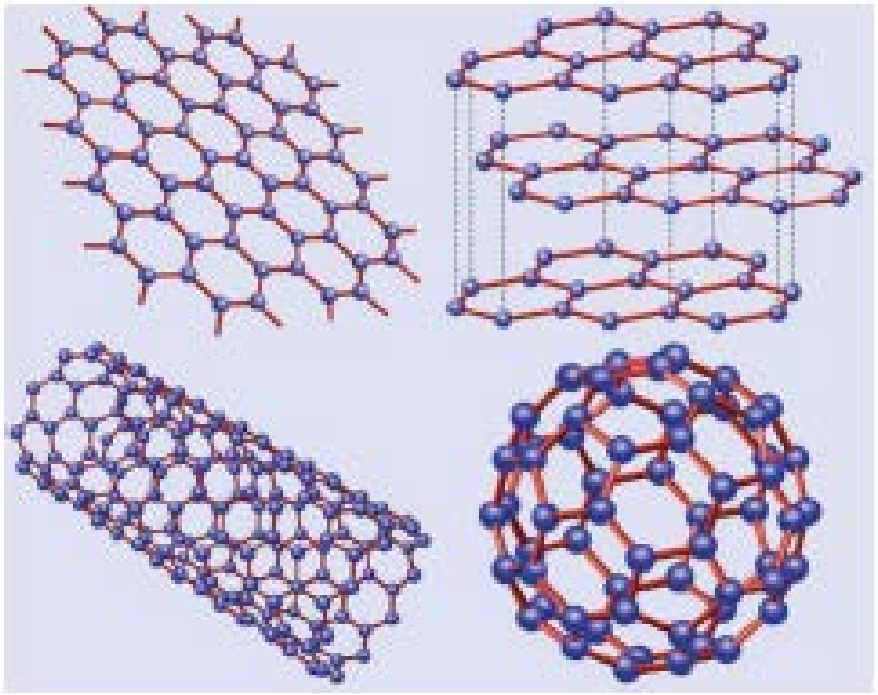
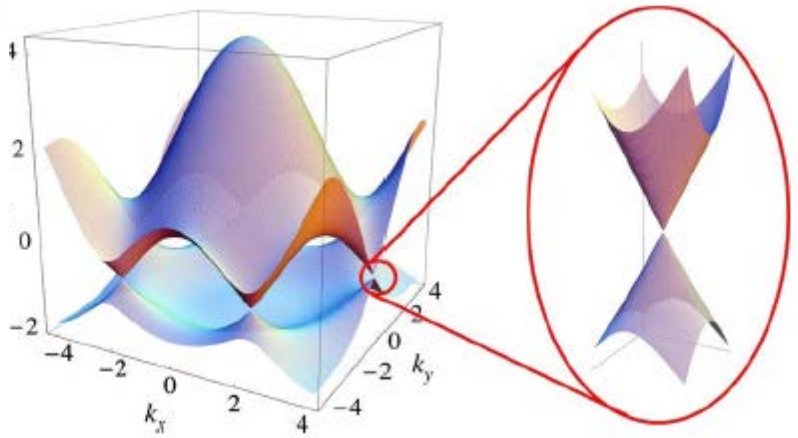
Graphene : Ultimate material ?





A.H.Castro Neto, et al., Rev.Mod.Phys. B. 81(2009), 109.

Mobility > 200,000cm^2/Vs

K.I.Bolotina, et al., solid state commun. 146(2008), 351.

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Summary

- **Cloud computing and storage data explosion lead to the large power consumption of IT facilities worldwide. Sensor Network system requires vast numbers of low power sensor nodes. Measures for the dramatic reduction of power consumption of LSIs are quite important.**

- **Novel approach such as 3D channel structure, strain introduction, parasitic resistance reduction as well as application of new channel material is effective to meet the demands through the reduction of the power supply voltage of LSIs.**

- **Further research and development of this field is indispensable for the evolution of very low power electric system throughout the globe.**

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